In the Specification:

Please amend the paragraph beginning on page 2, line 23 as follows:

One cause of tuning delays when a conventional PLL-based synthesizer is first powered On or changes operating frequencies is that the tuning time is not determinable or predictable because the initial phase is unknown and/or random. That is, the synthesizer ~~make~~ may take a relatively short time, or a relatively long time beyond a maximum channel-to-channel time, to lock onto the desired frequency and phase.

Please amend the paragraph beginning on page 6, line 34 as follows:

Typically, slave devices 204 keep their receivers powered On to detect and receive transmissions from a master device 202. Keeping a slave device's receiver powered On wastes precious power if the master device 202 only ~~transmit~~ transmits during known periodic time slots as illustrated in Figure 2B.

Please amend the paragraph beginning on page 18, line 9 as follows:

The synthesizer 302 may then generate a second Channel Select signal ~~522~~ 622 at time t3' to change from the previous operating frequency to a new operating frequency. This second Channel Select signal 622 may occur after the reference frequency divider 412 signal and the main frequency divider 410 signal are coarsely or substantially, but not necessarily completely, locked in phase. This reduces the time it takes to jump to the next channel.